J Electroceram (2010) 24:153–160
DOI 10.1007/s10832-008-9550-y

Substrate effect on the electrical properties of sputtered YSZ thin films for co-planar SOFC applications

Sung Moon Kim · Ji-Won Son · Kyung-Ryul Lee · Hyoungchul Kim · Hae-Ryoung Kim · Hae-Weon Lee · Jong-Ho Lee

Received: 9 May 2008 / Accepted: 11 September 2008 / Published online: 7 October 2008

Abstract The physical and electrical properties of sputtered YSZ thin films on various substrates were investigated. The in-plane electrical properties of the films were measured for evaluating YSZ thin film for co-planar SOFC electrolytes. The conductance measured on YSZ over Si substrates was significantly affected by the buffer layer thickness and exhibited higher values than that of YSZ on sapphire. This indicates that electrical leakage occurred through the substrate when Si substrates were utilized. Nevertheless, pure ionic conduction was observed in YSZ/sapphire regardless of the film thickness. It implies that much care should be taken for the selection of substrate materials in measuring or utilizing in-plane conductivity, especially for high temperature applications.

Keywords YSZ thin film · Sputtering · Electrical conductivity · Substrate effect · Co-planar SOFC

1 Introduction

In the past decade, solid oxide fuel cells (SOFCs) have drawn increasing interest as the next generation of power sources due to their high power density, efficiency, and environmental friendliness. Most of the research efforts in SOFCs have focused on the applications of several of the kW levels, e.g., residential power generation (RPG) and auxiliary power units (APU) of automobiles. Recently, however, much attention has been given to miniaturized SOFCs for portable and integrated power sources. This is because current micro power sources, such as rechargeable batteries, cannot keep pace with the growing power demand of advanced portable electronic devices [1–3]. Since a micro-SOFC has much higher power and energy densities over current portable power sources, it is expected to become the next-generation portable and mobile power source.

However, simple size reduction of conventional SOFCs would not satisfy the requirements for portable applications. As the dimension of the cell components reduces, alternate manufacturing methods should be employed, since traditional bulk processes have their limitation for fabricating micro-size components [4]. Thus, micro-fabrication techniques appear to be essential for developing fuel cells in small dimensions. Among them, thin film deposition of electrolytes has been studied by many researchers for several distinctive advantages. The decrease of the ohmic resistance due to the thickness reduction [5] is probably the most significant reason. Also, the possibility of utilizing the increase of electrical conduction through the nano-size effect [6–9] can be another example. However nano-size effect is still under debate since it was mostly observed in thin film YSZ [6, 7, 9] than in nano-crystalline bulk materials [10].

There have been many trials to construct a conventional vertical positive-electrolyte-negative (PEN) structured SOFCs either by deposition of thin electrolyte films on porous substrates [5, 11, 12], or employing back-etching after deposition of thin electrolyte film on dense substrates [13]. For using porous substrates, films with a substantial thickness (>>1 μm) need to be deposited to obtain completely impermeable electrolytes onto porous substrates containing approximately micrometer sized pores. For back-etched structures, mechanical frailty of the free standing cell membrane can be a concern.

S. M. Kim · J.-W. Son (✉) · K.-R. Lee · H. Kim · H.-R. Kim · H.-W. Lee · J.-H. Lee
Center for Energy Materials Research,
Korea Institute of Science and Technology,
P.O. Box 131, Cheongryang,
Seoul 130-650, Korea
e-mail: jwson@kist.re.kr

In this regard, a co-planar type single chamber SOFC (SC-SOFC) is an attractive application for vacuum deposited thin films. In the co-planar SC-SOFC, both the anode and the cathode are placed on the same surface of the electrolyte [14, 15]. In this design, electrolytes can be deposited on dense supports or can have a sufficient thickness to become a support itself. Therefore, the mechanical strength of the cell can be secured. And since the electrodes are deployed on a common plane, the co-planar SC-SOFC design is compatible with two-dimensional integration by using micro-fabrication [2], such as thin film deposition and patterning used in the IC fabrication. Moreover, a sealless design and higher thermal cycling resistance of a SC-SOFC are also beneficial aspects for portable and micro power applications [16].

However, for using YSZ as an electrolyte of co-planar type SOFCs, it is important to understand its physico-chemical properties in the in-plane configuration and under the effects of the substrates at the operation temperature range of SOFC (>500 °C), since in this design the vacuum deposited thin film electrolytes are fabricated on substrates and the properties of the thin film would be significantly affected by the substrate. Especially, when employing micro-fabrication, the most considered substrate is silicon. Hence there are previous reports that used silicon base substrates to characterize thin film SOFC components by using in-plane electrode configurations [1, 17–19]. However, the effect of the substrate and/or buffer layer has not been thoroughly discussed. In ref. [17], Zhang et al. considered the higher conductivity value was sorely from the thin film, but Bieberle-Hütter et al. [18, 19] mentioned the possibility of electrical leakage through more conductive substrates, even with a 1 μm-thick dense buffer layer.

For clarifying of this like confusion, in this study we measured the electrical properties of YSZ thin films on various substrates, especially Si-base substrates with various buffer layers and compared them with that of the YSZ films on insulating substrates. From this investigation we checked the viability of vacuum deposited thin film electrolytes in co-planar type SOFC designs. Further concerning points and/or key guidelines for measuring and utilizing the properties of thin film electrolytes in in-plane configuration are addressed as well.

2 Experimental procedure

YSZ thin films with various thicknesses from ~180 to ~900 nm were deposited on several different varieties of substrates by using RF sputtering. An 8 mol% Y_2O_3–ZrO_2 (8YSZ) sintered target was used for sputtering and RF power was 200 W during the deposition. The substrate temperature was 575 °C and the ambient pressure was ~12 mTorr at an O_2/Ar gas ratio of 0.1 (3/30 sccm). The measured growth rate of YSZ thin films by SEM cross-sectional observation was approximately 1 nm/min. Film composition, orientation, and microstructures were characterized by AES and EDS, XRD, and SEM, respectively.

For electrical conductivity measurements, two electrodes were formed by screen printing Au paste on the surface of the YSZ thin films (two-probe set-up). The printed electrodes were fired at 800 °C for 1 h. A schematic of dimensions and configuration of the electrodes is shown in Fig. 1. The Au electrode width (W) was 0.2 cm, the length (L) was 1 cm, and the gap between the electrodes (G) was 0.04 cm. AC impedance measurements were performed at a temperature range of 500–850 °C by using Solartron 1260 and 1296. The AC amplitude was 100 mV and the frequency range was 1×10^6–0.1 Hz.

For investigating influences of the substrates, we first deposited 900 nm-thick YSZ thin films on silicon substrates with various buffer layers, as well as on a sapphire substrate. Afterwards, we compared the measured conductance of these samples. Three different silicon substrates with different buffer layers were used: one with 100 nm Al_2O_3 buffer layer; another with 1 μm SiO_2 layer; and, the third with 100 nm Al_2O_3 over 1 μm SiO_2 layer. These substrates are denoted as AS, SS, and ASS, respectively. The 1 μm-thick SiO_2 layer of SiO_2/Si wafer (i-Nexus, Inc., Korea) was prepared by wet thermal oxidation of (100)-oriented p-type Si wafers (Single Crystal Substrate of America, Inc., USA). 100 nm-thick Al_2O_3 layers (INOSTEK, Korea) were formed by a sol–gel method over Si and SiO_2/Si wafers. The description of samples prepared and their denotations are listed in Table 1. The effect of the film thickness was examined in the YSZ films deposited on c-cut ((0001)-oriented) sapphire substrates (Kyocera, Japan) with rms roughness of ~1 Å (C-Sap). The characteristics of ionic conduction were also studied on these specimens by varying oxygen partial pressure.

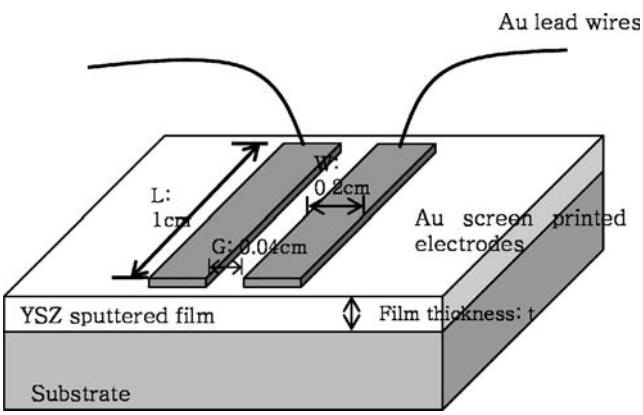

Fig. 1 Schematic of electrode configuration

Table 1 Denotation of substrate types and YSZ film thicknesses examined.

Denotation	Substrate type	YSZ film thickness (nm)
AS	Al_2O_3 (100 nm)/Si	900
SS	SiO_2 (1 μm)/Si	900
ASS	Al_2O_3 (100 nm)/SiO_2 (1 μm)/Si	900
C-Sap	Sapphire with 1 Å surface roughness	180
		360
		900

3 Results and discussion

3.1 Physical properties of sputtered YSZ thin films

In Fig. 2, XRD results of YSZ samples are displayed. The results of 900 nm thick YSZ films on Si substrates with various buffer layers (AS, SS, ASS) are shown in Fig. 2(a), and those of YSZ films with various thicknesses on c-cut sapphire substrates (C-Sap) are shown in Fig. 2(b). It has been determined that the YSZ films have a strong (111) texture regardless of the buffer layer on the Si substrate. Also, the films on c-cut sapphire substrates have the same tendency of the orientation for all thicknesses examined. The surface morphology and the cross-sectional microstructure of the film on SS are shown in Fig. 3(a) and (b), respectively. The films deposited on other Si-base substrates, AS and ASS, have a similar microstructure. The film consists of several tens of nanometer grains and has a pronounced columnar grain structure. The film deposited on the sapphire substrates has a similar surface morphology as shown in Fig. 3(c), and also the cross-sectional microstructure shown in Fig. 3(d) exhibits a columnar structure. However, the column boundaries are not as pronounced as that of Fig. 3(b). Similar results have been reported in ref. [8]. Although there is a slight difference in the cross-sectional microstructures, we can conclude the sputter deposited YSZ films are polycrystalline films with a strong (111) texture regardless of the substrate types based on the surface morphologies and the XRD results.

The atomic ratios of Y in the films were analyzed by using AES and EDS, and Y to (Y+Zr) ratios were measured as 0.178 and 0.166, respectively. The calculated Y/(Y+Zr) ratio of 8YSZ is 0.148, thus the YSZ film is slightly Y_2O_3 excess in composition than 8YSZ.

3.2 Substrate effects on electrical property measurement of YSZ

In this section, we compare the electrical conducting properties of 900 nm thick YSZ thin films deposited on silicon substrates with various buffer layers (AS, SS, ASS)

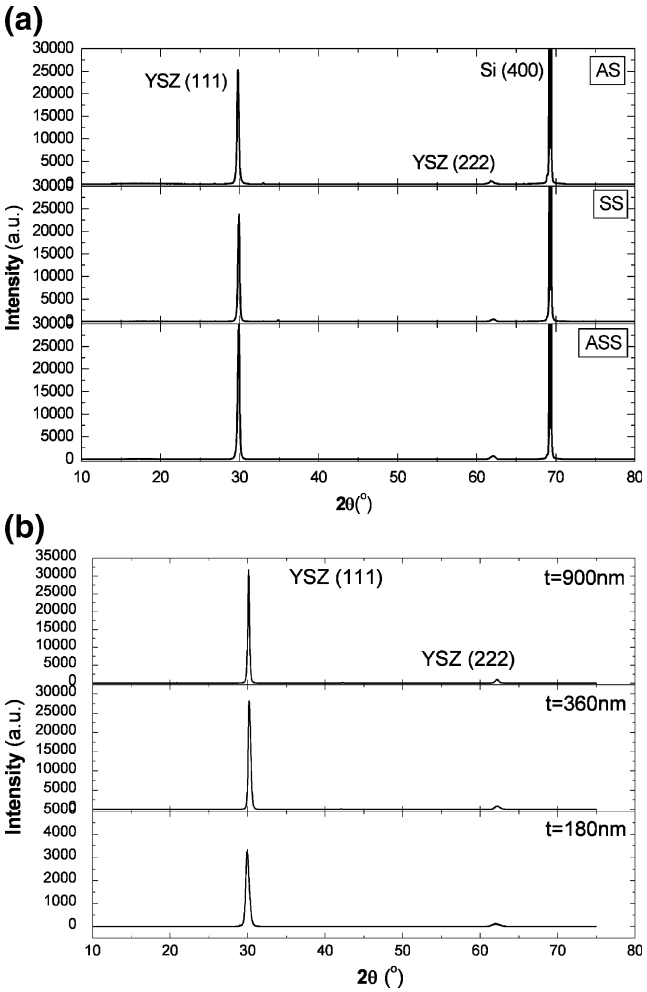

Fig. 2 XRD results from (**a**) 900 nm YSZ thin films on Si-base substrates with various buffer layers; and (**b**) YSZ with different thicknesses on sapphire substrates (C-Sap) (on AS, Al_2O_3 (100 nm)/Si substrate; ASS, Al_2O_3 (100 nm)/SiO_2 (1 μm)/Si substrate; SS, SiO_2 (1 μm)/Si substrate; C-Sap, c-cut sapphire substrate)

and a sapphire substrate (C-Sap). As mentioned previously, the YSZ film deposition conditions and all the electrode conditions such as Au electrode configurations and the electrode thermal treatment condition were identical for each sample. We first use the 1/R value of each sample instead of the conductivity σ for the comparison of conducting properties. It is because that the precise definition of the electrode area (A) and length (l) of the conducting materials in the on-plane electrode configuration for deducing $\sigma = \frac{1}{R} \times \frac{l}{A}$ is not as straightforward as that of a face-to-face electrode configuration. We will revisit this issue in the later section.

In Fig. 4, the impedance spectrum measured at 850 °C on 900 nm YSZ over ASS substrate is shown. Other measurements at different temperatures and/or different samples showed similar spectra, which exhibited a semicircle arc at the high frequency range coming from the sample, and another big low frequency arc due to the

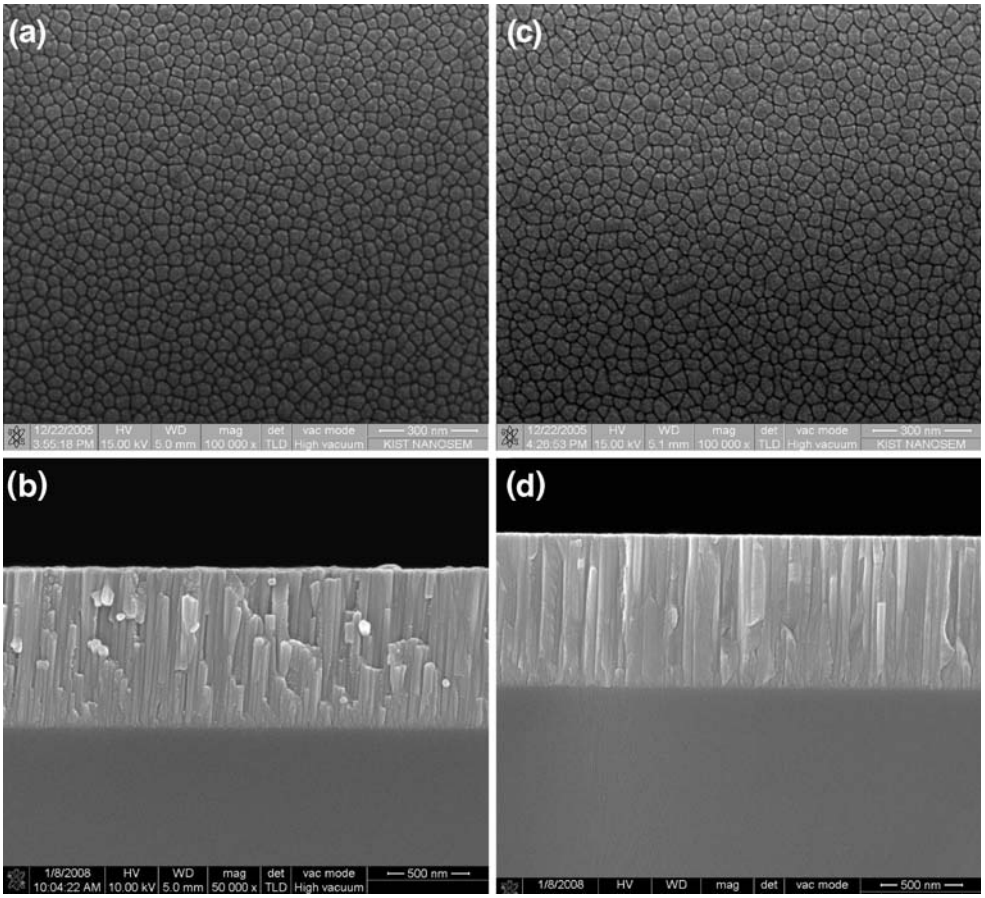

Fig. 3 Plan-view and cross-sectional SEM micrographs of 900 nm YSZ on (**a**, **b**) SS (SiO_2/Si); and on (**c**, **d**) C-Sap

electrode reaction. The sample resistances R were determined by the fitting the high frequency arc and taking the value of the intersection on the real axis as shown in Fig. 4. In Fig. 5, the $1/R$ values measured for each sample are compared. Considering that all samples have identical electrode configurations and thin film thicknesses, the $1/R$ values can be directly related to the conductivity of each sample. The $1/R$ of 900 nm YSZ on AS is about one order

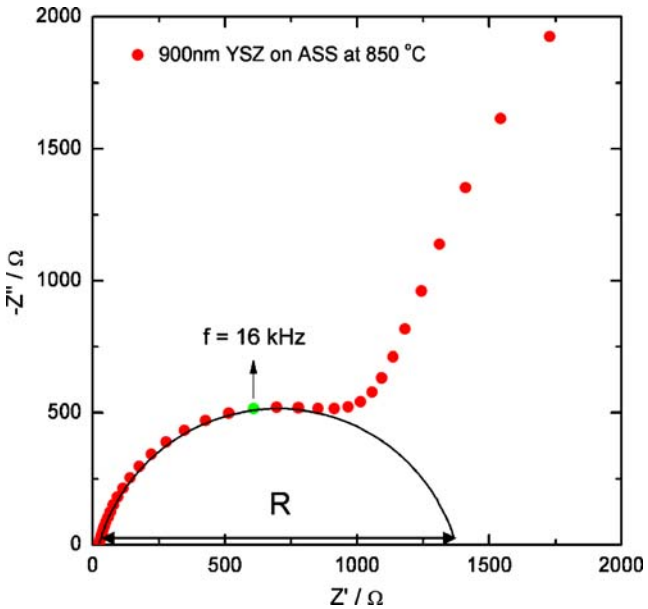

Fig. 4 Impedance spectrum of 900 nm YSZ on ASS (Al_2O_3/SiO_2/Si) at 850 °C, in air

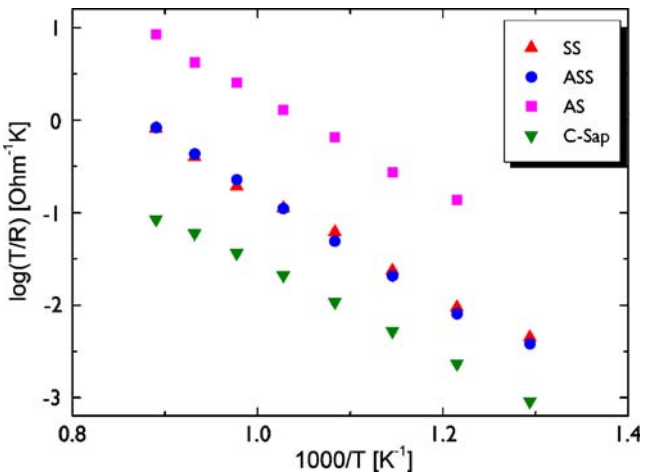

Fig. 5 Comparison of $1/R$ values of 900 nm YSZ on various substrates (on AS, Al_2O_3 (100 nm)/Si substrate; ASS, Al_2O_3 (100 nm)/SiO_2 (1 μm)/Si substrate; SS, SiO_2 (1 μm)/Si substrate; C-Sap, c-cut (0001) sapphire substrate)

of magnitude higher than those of YSZ on ASS and SS. Again, the $1/R$ of YSZ on C-Sap is about one order of magnitude lower than those of YSZ on ASS and SS. In each case the activation energies are 1.18, 1.1, 1.08, and 1 eV for films on ASS, AS, SS, and C-sap, respectively.

The reported properties of the films deposited by physical vapor deposition methods [8, 9] can be compared with our results. In those reports, YSZ with thickness over several hundred nanometers (~210 nm [9]) exhibited conductivity close to bulk. Those YSZ films were deposited on insulators such as sapphire and MgO single crystal substrates. Therefore, we postulate that the electrical properties of ~1 μm-thick YSZ on C-Sap reflect the genuine YSZ film conductivity without any artifact. On the other hand, the higher $1/R$ values of the films over Si-base substrates seem to result from the substrate effect which might be correlated with the thickness of the buffer layers over Si. As explained in Table 1, ASS and SS have different buffer layer configurations and different interfaces between thin film layers, whereas the thickness of the buffer layers are in a similar range (1,100 and 1,000 nm, respectively). In these cases, ASS and SS exhibited similar conductance values as shown in Fig. 5. However, the conductance values of AS and ASS show a significant difference due to the great difference in buffer layer thickness (100 and 1,100 nm), whereas they have the same interfaces between YSZ thin film layers and substrate surfaces. From these results, we can infer that the apparent conductance of YSZ film on Si substrate is primarily dependent on the thickness of the buffer layers.

A more intuitive explanation for the apparent high conductance of YSZ films might be the current passing through the high conductive Si-substrate. However, some sort of AC coupling effect without any current leakage might be another possibility, inducing apparent high conductance of YSZ films. In AC coupling, which is also known as capacitive coupling, AC signals can be coupled by capacitors in series while DC currents are blocked [20]. This capacitive coupling can be an accidental effect in AC impedance spectroscopy. Under this condition, AC coupled signals can result in the relatively higher conductance measured in AC impedance spectroscopy.

In order to verify the exact Si-substrate effect, we measured DC conductivity and compared it with AC impedance. If the AC measurement picked up the coupled signals due to the capacitive coupling effect, the resistance measured by DC should be higher than that of the AC measurement because the DC current should be blocked with insulating buffer layers. According to our comparison between the resistance from DC two-probe and AC impedance measurements, the DC resistance was well matched with the total R value (bulk+electrode) of AC within the experimental error (less than 10%). Based on these observations, we believe that the actual faster conducting path resides underneath buffer layers, i.e., in silicon part of the substrate. The electrode configuration we used should have acknowledged such a signal. It is quite surprising that even the buffer layer with the thickness exceeding 1 μm could not completely block the current leak through the Si layer at this temperature range, knowing that YSZ on SS and ASS have higher conductance than those of YSZ on C-Sap.

We suspect that the electrode area of the Au electrodes ($W \times L$ refer Fig. 1) was excessive compared with the thickness of the YSZ film and the buffer layers. Thus, current paths underneath this wide electrode would penetrate deeply into the sample structure, even down to the Si part of the substrate. To check the feasibility of this assumption, we roughly calculated the resistance for two distinctive electrical paths, shown in Fig. 6. Path A represents conduction through YSZ thin film by the shortest conduction path, and path B shows conduction penetrating YSZ and buffer layers and passing through Si substrates. If we assume that the entire thickness t_f is active for the conduction, the resistance for Path A is:

$$R_A = \frac{l}{A}\rho_{YSZ} = \frac{G}{L \times t_f}\rho_{YSZ}. \quad (1)$$

For Path B, if we assume the resistance of Si is negligible compared with other resistances, then:

$$R_B = R_{\text{thru Si}} + 2 \times R_{\text{thru YSZ and Buffer}} \approx 2 \times R_{\text{thru YSZ and Buffer}} = 2 \times \left(\frac{t_f}{W \times L}\rho_{YSZ} + \frac{t_b}{W \times L}\rho_{\text{buffer}}\right) \quad (2)$$

where G=0.04 cm; W=0.2 cm; L=1 cm in our measurement configuration. Here we put t_f and t_b as 1 μm, and ρ_{YSZ} is ~65 Ωcm at 700 °C. Assuming we have a single SiO_2 buffer layer which has $\rho_{\text{buffer}} \sim 10^6$ Ωcm at 700 °C [21], then $R_A = 2.6 \times 10^4$ Ω and $R_B \sim 10^3$ Ω, respectively. This is an order of magnitude difference; therefore it is highly possible that the electrical leakage occurred by penetrating YSZ and buffer layers down to Si-substrate at a high temperature. Others also suspected an electrical leakage happened through Si substrates with Si_3N_4 buffers, however, in this case the activation energies were reported much lower than 1 eV [18, 19]. It is unclear at this point why the

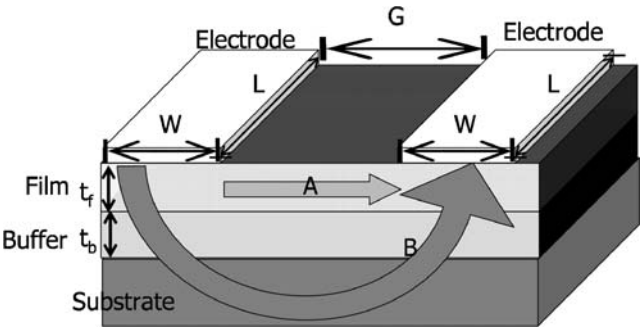

Fig. 6 Two distinctive conduction paths of specimens, without electrical leakage to substrate (*Path A*) and with leakage (*Path B*)

activation energy difference was observed between our case and other's. However, both results imply that for measuring or utilizing the sole in-plane electrical properties of the films deposited on Si-base substrates, reducing electrode pattern sizes or selecting proper buffer layer thicknesses should be seriously considered.

3.3 Electrical properties of YSZ thin films on sapphire substrates

As in the previous section, to rule out the interference from the conductive substrate, it is better to avoid Si-base substrates in our electrode geometry. Thus, sapphire substrates were used for further investigation. In Fig. 7(a), measured $1/R$ values of YSZ films with different thicknesses on C-Sap are shown. As one can easily expect, the conductance of thin films would increase with the thickness of the thin films, since the conduit for electrical current is widened in the in-plane measurement. However, as previously mentioned, defining the electrode area (A) and length (l) for deducing $\sigma = \frac{1}{R} \times \frac{l}{A}$ is not a trivial problem in the in-plane measurement. For in-plane measurement as shown in Fig. 1, the actual portion of W and t contributing to conduction are dependent with each other. For example, as the thickness of the electrolytes (t) increases, a participating portion of electrode width W can increase and thus effective length of conducting volume of the electrolyte would also increase (Kim et al., in preparation). In ref. [22], we could also observe that the effective electrolyte volumes can be significantly different for two extremely different electrolyte thicknesses. During our measurement, we had this concern for the electrolyte thickness for most thin film applications, i.e. <1 μm. Therefore, we varied the thin film thickness and measured the electrical properties under the same electrode configuration. Then we normalized the $1/R$ values with t. The results are shown in Fig. 7(b). Since the normalized values fell in one line, it is shown that the contribution of W does

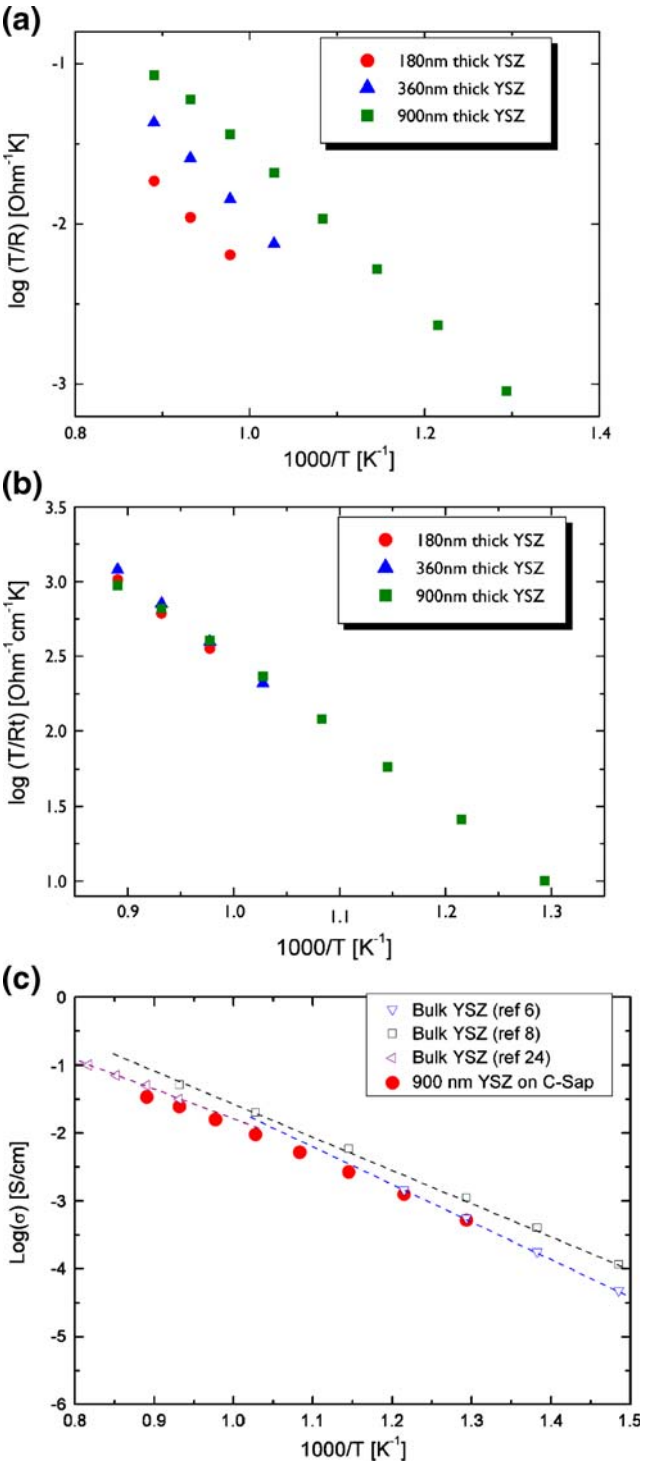

Fig. 7 (**a**) $1/R$ values of YSZ of various thicknesses on C-Sap; (**b**) $1/R$ values normalized with film thicknesses; (**c**) estimated conductivity of 900 nm YSZ on C-Sap compared with reference data [6, 8, 23]

not change in the thickness range of <1 μm in our configuration. In fact, the contribution of W appeared to be minute and the length of the conducting volume (l) would be close to G (0.04 cm) in this configuration, according to

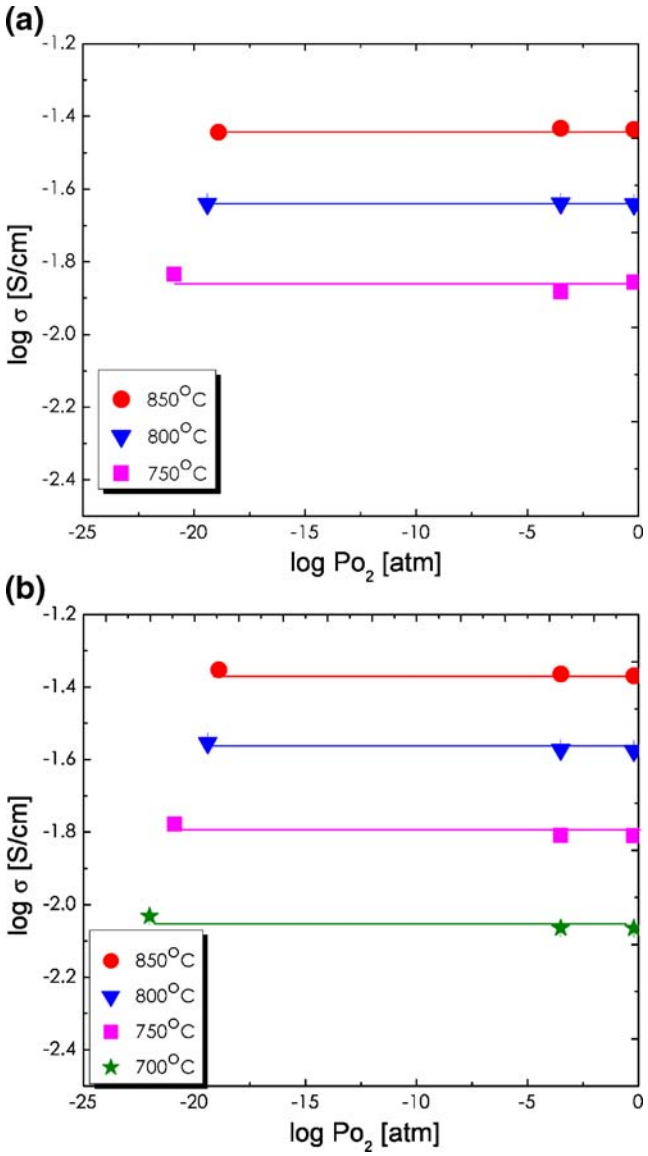

Fig. 8 σ vs. Po_2 of (**a**) 180 nm YSZ on C-Sap; and (**b**) 360 nm YSZ on C-Sap

our simulation (Kim et al., in preparation). This also corresponds to the regime where the assumption that $G \sim l$ and the electrode area $A = t \times L$ is valid when G >> t [2]. Hence, we calculated the conductivity of 900 nm YSZ on C-Sap with the applied dimensions of $A = t \times L$ and $l=G$. The result is displayed in Fig. 7(c). When compared with the reference value measured in bulk [6, 8, 23], the activation energy was in a similar range and the calculated σ of the film on C-Sap was similar or slightly lower than that of the bulk. In ref. [8] and [9], the σ of YSZ films also exhibited slightly lower values than those of bulk references in the thickness range close to 1 μm. Thus, the lower σ value estimated could come from the properties of the thin films on substrates, which can be related to the stress and strain by thermal or lattice mismatch with substrates, interface formation to substrates, etc. However, we should not completely exclude the possibility of defining effective electrode dimensions was not precisely reflecting the actual electrode dimensions.

For identifying the nature of the electrical conduction in the YSZ films, we measured the film's conductivity as a function of oxygen partial pressure. In Fig. 8, the conductivities measured at various temperatures on 180 and 360 nm-thick YSZ samples deposited on C-Sap are exhibited. The measurements of the oxygen partial pressure dependence of σ were performed at the temperatures of 700, 750, 800, and 850 °C for both samples. For 180 nm YSZ, though, it was difficult to measure the electrical property at 700 °C since the conductance was too low. At the temperatures that we could measure the electrical properties, it is clearly shown in Fig. 8 that the conductivity does not change at the range of $\sim 10^{-20} < Po_2 < 1$ atm, thus the electrical conductivity of the YSZ films appears to be ionic.

4 Conclusions

Sputtered YSZ thin films on various substrates were investigated for their physical and electrical properties. The co-planar type SC-SOFC was the application of the interest, thus the on-plane electrode configuration was employed to probe electrical properties. Highly (111) oriented 8YSZ thin films with a polycrystalline structure were obtained on substrates including Si with diverse buffer layers and sapphire. The conductance of the sample prepared on Si-base substrates exhibited higher values than that of the sample prepared on sapphire. Since the conductance decreased with the buffer layer thickness, we believe that electrical leakage occurred. Therefore, care should be taken for the selection of proper buffer layer thicknesses and electrode dimensions to use Si-base substrates in this configuration, especially for high temperature applications. For the samples prepared on sapphire substrates, the conductance normalized by the film thickness fell in a single line when plotted vs. $1/T$. This indicates that the contribution of the width of the on-plane electrode, W, did not change in the thickness range we investigated; and, the film thickness t is one of the major contributors for area A in conductivity estimation. Also, ionic conduction was confirmed in YSZ deposited on sapphire substrates since the conductivity did not depend on oxygen partial pressure.

Acknowledgment This work has been supported by the Institutional Research Program and NRL Program of Korea Institute of Science and Technology (KIST).

References

1. J.L. Hertz, H.L. Tuller, J. Electroceramics **13**, 663 (2004)
2. J. Fleig, H.L. Tuller, J. Maier, Solid State Ion. **174**, 261 (2004). doi:10.1016/j.ssi.2004.07.035
3. A. Bieberle-Hutter et al., J. Power Sources **177**, 123 (2008). doi:10.1016/j.jpowsour.2007.10.092
4. R. O'Hayre, Ph.D. Dissertation, Stanford University (2004)
5. L.R. Pederson, P. Singh, X.-D. Zhou, Vacuum **80**, 1066 (2006). doi:10.1016/j.vacuum.2006.01.072
6. I. Kosacki, T. Suzuki, V. Petrovsky, H.U. Anderson, Solid State Ion **136**–**137**, 1225 (2000). doi:10.1016/S0167-2738(00)00591-9
7. I. Kosacki, C. Rouleau, P.F. Becher, J. Bentley, D.H. Lowndes, Solid State Ion. **176**, 1319 (2005). doi:10.1016/j.ssi.2005.02.021
8. J.H. Joo, G.M. Choi, Solid State Ion. **177**, 1053 (2006). doi:10.1016/j.ssi.2006.04.008
9. A. Karthikeyan, C. Chang, S. Ramanathan, Appl. Phys. Lett. **89**, 183116 (2006). doi:10.1063/1.2385211
10. H.L. Tuller, Solid State Ion. **131**, 143 (2000). doi:10.1016/S0167-2738(00)00629-9
11. L.C. De Jonghe, C.P. Jacobson, S.J. Visco, Annu. Rev. Mater. Res. **33**, 169 (2003). doi:10.1146/annurev.matsci.33.041202.103842
12. B. Hobein, F. Tietz, D. Stover, M. Cekada, P. Panjan, J. Eur. Ceram. Soc. **21**, 1843 (2001). doi:10.1016/S0955-2219(01)00127-3
13. H. Huang, M. Nakamura, P. Su, R. Fasching, Y. Saito, F.B. Prinz, J. Electrochem. Soc. **154**, B20 (2007). doi:10.1149/1.2372592
14. T. Hibino, K. Ushiki, Y. Kuwahara, Solid State Ion. **91**, 69 (1996). doi:10.1016/S0167-2738(96)00437-7
15. M. Yano, A. Tomita, M. Sano, T. Hibino, Solid State Ion. **177**, 3351 (2007). doi:10.1016/j.ssi.2006.10.014
16. Z. Shao, S.M. Haile, J. Ahn, P.D. Ronney, Z. Zhan, S.A. Barnett, Nature **435**, 795 (2005). doi:10.1038/nature03673
17. Z.W. Zhang, S. Jin, Y. Yang, G.B. Li, S.J. Tian, J.T. Jia et al., Appl. Phys. Lett. **77**(21), 3409 (2000). doi:10.1063/1.1328099
18. A. Bieberle-Hütter, M. Søgaard, H.L. Tuller, Solid State Ion. **177**, 1969 (2006). doi:10.1016/j.ssi.2006.06.017
19. A. Bieberle-Hütter, J.L. Hertz, H.L. Tuller, Acta Mater. **56**, 177 (2008). doi:10.1016/j.actamat.2007.09.006
20. M.N. Horenstein, *Microelectronic Circuits and Devices* (Prentice Hall, New Jersey, 1996), p. 426
21. G.V. Samsonov (ed.), *The Oxide Handbook* (IFI/Plenum, New York, 1982), p 202
22. J.L. Hertz, H.L. Tuller, Solid State Ion. **178**, 915 (2007). doi:10.1016/j.ssi.2007.04.003
23. J. Kim, R.N. Blumenthal, J. Electrochem. Soc. **136**(10), 2867 (1989). doi:10.1149/1.2096302